While reliability of the power semiconductor device is improved by using Al/SiC and Cu/Mo for the metal base plate, these materials have a disadvantage of being more costly than Cu.

Please replace the paragraph beginning on page 2, lines 8-12, with the following text:

When an Al alloy is used as the material for the circuit pattern and the lower pattern, instead of Cu, the resistance to cracks of the insulating substrate can be improved. However, cracks caused in the soldering layer in the above-noted early stage due to a temperature cycle are not eliminated by this alternative.

Please replace the paragraph beginning on page 2, lines 13-17, with the following text:

Moreover, when the lower pattern is made of an Al alloy having a thickness of 0.4 to 0.5 mm, electrical resistance is increased as compared with the electrical resistance of a lower patter made of a Cu alloy. This increase in electrical resistance results in an increase in heat resistance of the power semiconductor device as a whole, to thereby reduce the heat dissipation capacity of a semiconductor element to be mounted on the insulating substrate.

Please replace the paragraph beginning on page 2, line 18 to page 3, line 2, with the following text:

Further, as the thickness of the soldering layer has been arbitrarily set, and there has been no concern as to the soldering layer being defined to have a nonuniform thickness, the insulating substrate may be inclined at a junction between the lower pattern and the metal base plate, causing heat resistance to increase. Consequently, it is probable that a balance between target heat resistance and resistance of the soldering layer to cracks may be lost, resulting in the problems of increased dispersion of a quality, change of design and decreased tolerance of design. A further problem is that the above-noted cracks due to a temperature

cycle are likely to occur in the soldering layer at its corner portions that are of a thinned thickness in the above-noted early stage. This problem may result in increased heat resistance, to thereby destroy the power semiconductor element.

Please replace the paragraph beginning on page 3, lines 5-14, with the following text:

A first aspect of the present invention is directed to a power semiconductor device, comprising: a ceramic substrate having a thickness of 0.5 to 1 mm; a circuit pattern made of an aluminum alloy and provided on an upper main surface of the ceramic substrate and having a thickness of 0.4 to 0.6 mm on which a power semiconductor element is held; a lower pattern made of the aluminum alloy provided entirely on a lower main surface of the ceramic substrate opposite to the upper main surface; a metal base plate of a copper alloy having a thickness of 3.5 to 5.5 mm opposes the lower pattern; and a soldering layer provided between an entire surface of the lower pattern and the metal base plate for forming a joint therebetween.

Please replace the paragraph beginning on page 3, lines 15-24, with the following text:

A second aspect of the present invention is directed to a power semiconductor device, comprising: a ceramic substrate having a thickness of 0.5 to 1 mm; a circuit pattern made of an aluminum alloy and provided on an upper main surface of the ceramic substrate with a thickness of 0.4 to 0.6 mm for holding a power semiconductor element thereon; a lower pattern formed of a metalized layer having a thickness of 0.1 mm or less and provided entirely on a lower main surface of the ceramic substrate opposite to the upper main surface; a metal base plate made of a copper alloy having a thickness of 3.5 to 5.5 mm opposite to the lower pattern; and a soldering layer having uniform thickness of 50 to 400 μm is provided

between an entire surface of the lower pattern and the metal base plate for forming a joint therebetween.

Please replace the paragraph beginning on page 4, lines 3-5, with the following text:

According to the first aspect of the present invention, it is possible to provide a power semiconductor device excellent in heat dissipation capacity and heat cycle.

Please replace the paragraph beginning on page 4, lines 6-9, with the following text:

According to the second aspect of the present invention, as the lower pattern is formed of the metalized layer, the soldering layer as well as the lower pattern can be reduced in thickness. As a result, it is possible to provide an inexpensive power semiconductor device excellent in heat dissipation capacity and productivity.

Please replace the paragraph beginning on page 4, lines 10-16, with the following text:

According to the third aspect of the present invention, it is possible to prevent the ceramic substrate from being inclined at a junction between the lower pattern and the metal base plate. Further, uniform spacing between the lower pattern and the metal base plate can be ensured. In addition, the thickness of the soldering layer is made uniform to enable the soldering layer to be reduced in thickness. As a result, excellent productivity and high cost reduction can be obtained.

Please replace the paragraph beginning on page 4, lines 17-20, with the following text:

It is an object of the present invention to provide a power semiconductor device having a circuit pattern and a lower pattern made of an Al alloy for cost reduction and enabling reduction in heat resistance and improvement in resistance of a soldering layer as to cracking during a heat cycle.

Please replace the paragraph beginning on page 5, line 5, with the following text:

a11 Fig. 3 is a graph showing comparative data as to the present invention.

Please replace the paragraph beginning on page 5, lines 8-9, with the following text:

a12 Fig. 1 is a cross-sectional view illustrating a power semiconductor device that is commonly applicable to the preferred embodiment described later.

Please replace the paragraph beginning on page 6, lines 11-14, with the following text:

a13 Fig. 3 is a graph showing comparative data as to the present invention. A group of t_2 lines enclosed by L1 refers to dependence of distortion ϵ (absolute number) occurring in the soldering layer 8C due to a heat cycle on the thickness t_3 of soldering layer 8C. The group of lines t_2 enclosed by L2 refers to dependence of heat resistance R_{th} ($°C/W$), on the thickness t_3 of the soldering layer 8C.

Please replace the paragraph beginning on page 6, lines 15-17, with the following text:

a14 The heat cycle requires temperature ranging from -40 to 125°C. The target number of times of heat cycles is 1000 to 1500 cycles in power modules for electric railways and automobiles requiring high reliability.

Please replace the paragraph beginning on page 6, line 18 to page 7, line 4, with the following text:

a15 In the group of t_2 lines enclosed by L1 (L11, line L12, line L13 and line L14) show the selection of the thickness t_2 of the lower pattern 5 of 0.1 mm, 0.2 mm, 0.3 mm and 0.4 mm, respectively. In the group of t_2 lines enclosed by L2 (line L21, line L22, line L23 and line L24) show the selection of the thickness t_2 of the lower pattern 5 of 0.1 mm, 0.2 mm, 0.3 mm and 0.4 mm, respectively. When Al foil is joined as the lower pattern 5 on the insulating

substrate 3 made of ceramics, a lower limit of the thickness t_2 may be around 0.1 mm. There occurs little fluctuation in lines L11, L12, L13, L14, L21, L22, L23 and L24 by the thickness of the metal base plate 1, the insulating substrate 3 and the circuit pattern 4 falling within the ranges thereof as mentioned above. For comparison, line L19 and line L29 defined by the circuit pattern 4 and the lower pattern 5 made of a Cu alloy are added to the group of t_2 lines enclosed by L1 and L2, respectively. More particularly, the circuit pattern 4 grows to a thickness of 0.3 mm and the lower pattern 5 grows to a thickness of 0.15 mm.

Please replace the paragraph beginning on page 7, lines 5-13, with the following text:

As the thickness t_3 of the soldering layer 8C increases and as the thickness t_2 of the lower pattern 5 decreases, the distortion ε occurring in the soldering layer 8C is reduced. In order to obtain the distortion ε that is smaller than the distortion occurring when a Cu alloy is used as the circuit pattern 4 and the lower pattern 5 (line L19), the thickness t_2 should be 0.1 mm (line L11) when an Al alloy is used as the lower pattern 5. However, in order to ensure the distortion ε in the soldering layer 8C has a value smaller than the illustrated permissible value ε_0, the thickness t_3 of the soldering layer 8C is required to be 100 μm or more when the thickness t_2 of the lower patter 5 is 0.1 mm.

Please replace the paragraph beginning on page 7, line 25 to page 8, line 8, with the following text:

In view of the foregoing, when both of the circuit pattern 4 and the lower pattern 5 are made of an Al alloy and when the thickness of the metal base plate 1, the insulating substrate 3 and the circuit pattern 4 fall within the ranges as mentioned above, for example, the thickness t_3 of the soldering layer 8C is set to fall within the range of 100 to 300 μm with the lower pattern 5 having the thickness t_2 of 0.2 mm or less to thereby control the distortion ε and the heat resistance R_{th} favorably. Therefore, a power semiconductor device excellent in

heat dissipation capacity and heat cycle can be provided. Further, the metal base plate 1 can be made of an inexpensive Cu alloy instead of costly Al/SiC and Cu/Mo.

Please replace the paragraph beginning on page 8, line 17 to page 9, line 4, with the following text:

Both of line L10 belonging to the group of t_2 lines L1 and line L20 belonging to the group of t_2 lines L2 are defined by the lower pattern 5 formed of a metalized layer. There occurs little fluctuation in lines L10 and L20 due to the thickness of the metal base plate 1, the insulating substrate 3 and the circuit pattern 4 under the condition that these thicknesses fall within the ranges thereof mentioned above. Such a metalized layer is formed using known metalizing techniques such as spraying or vapor deposition to provide a thickness of 0.005 to 0.1 mm, or preferably, 0.020 mm or less. As materials for the metalized layer, Mo-Mn (molybdenum-manganese) and W (tungsten) are applicable. Alternatively, a brazing material such as an Al-based material to be provided between the circuit pattern 4 and the insulating substrate 3 is applicable. In any case, in order to improve adhesion and wettability to the soldering layer 8C, it is desirable to plate the surface of the metalized layer, namely, the side to be joined onto the metal base plate 1, with Ni (nickel) plating.

Please replace the paragraph beginning on page 9, lines 15-18, with the following text:

In view of the foregoing, the thickness of the soldering layer 8C can be small according to this preferred embodiment. As a result, it is possible to provide an inexpensive power semiconductor device excellent in heat dissipation capacity and productivity.

Please replace the paragraph beginning on page 9, lines 20-23, with the following text:

As shown in Figs. 1 and 2, wire bumps 9 made of Al or the like are sandwiched between the lower pattern 5 and the metal base plate 1 to be in contact with the soldering layer 8C. A space between the metal base plate and the substrate 2 of semiconductor elements can be made uniform using these wire bumps 9.

Please replace the paragraph beginning on page 9, line 24 to page 10, line 4, with the following text:

The insulating substrate 3 can be thereby prevented from being inclined at a junction between the lower pattern 5 and the metal base plate 1. Further, uniform spacing between the lower pattern 5 and the metal base plate 1 can be ensured. In addition, the thickness of the soldering layer 8C is made uniform to enable the soldering layer 8C to be easily reduced in thickness. As a result, excellent productivity and effective cost reduction can be obtained.

Please replace the paragraph beginning on page 10, lines 5-8, with the following text:

In consideration of heat dissipation capacity and reliability, diameters of the wire bumps 9 are desirably about 50 to 400 μm. Consequently, it is clear that the wire bumps 9 are further applicable to the aforementioned first and second preferred embodiments.

IN THE CLAIMS

Please cancel Claims 4 and 7 without prejudice.

Please amend Claim 1 as shown in the attached marked-up copy to read as follows:

1. (Amended) A power semiconductor device comprising:

a ceramic substrate having a thickness of 0.5 to 1 mm;

a power semiconductor element;